CHA920001-003B

March 19, 2002

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/782,358 02/19/04

Tomoko Ogura et al.

STITCH AND SELECT IMPLEMENTATION IN TWIN MONOS ARRAY

INFORMATION DISCLOSURE STATEMENT

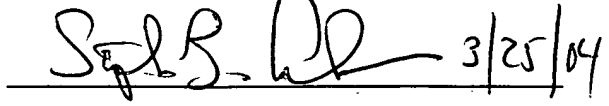
Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  3/25/04

U.S. Patent 6,255,166 to Ogura et al., "Nonvolatile Memory Cell, Method of Programming the Same and Nonvolatile Memory Array," discusses a high speed and low program voltage non-volatile memory cell, a programming method for same and a non-volatile memory array.

U.S. Patent 6,177,318 to Ogura et al., "Integration Method for Sidewall Split Gate MONOS Transistor," discloses a fabrication method for an electrically programmable read only memory device.

U.S. Patent 6,477,088 to Ogura et al., "Usage of Word Voltage Assistance in Twin MONOS Cell during Program and Erase," discusses a twin MONOS memory erase achieved by applying a positive bias to the bit diffusion and a negative bias to the control gate.

U.S. Patent 6,248,633 to Ogura et al., "Process for Making and Programming and Operating a Dual-Bit Multi-Level Ballistic MONOS Memory," describes a fast low voltage ballistic program, ultra-short channel, ultra-high density, dual-bit multi-level flash memory.

U.S. Patent 5,933,725 to Kirsch et al., "Word Line Resistance Reduction Method and Design for High Density Memory with Relaxed Metal Pitch," discloses a method and design for stitching polysilicon wordlines to straps formed of interconnected metal line segments formed in two or more metallization levels.

European Patent Application 0 487 468 A2 to Natale et al., "Flash-EPROM memory with single metal level, erasable per blocks of cells," discusses a FLASH-EPROM memory having a single metal architecture and wherein selectable sectors of the memory array may be separately erased.

U.S. Patent 5,973,953 to Yamashita et al., "Semiconductor Memory Device Having Improved Bit Line Structure," discusses a pair of adjacent common complementary data lines, namely the wiring between a pair of global I/O lines.

U.S. Patent 5,459,355 to Kreifels, "Multiple Layer Programmable Layout for Version Identification," discusses methods and apparatus for providing a multiple layer programmable layout which may be used for the identification of a version of an integrated circuit product.

An English Abstract of the following German Patent has been enclosed:

DE 198 24 209 A1 "Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen," discusses a method of offering specific array-end structures and their fabrication.

European Patent Application EP 0 871 221 A1 to Aldrich, "Filter capacitor for power bus," discusses an integrated circuit having a voltage source and a plurality of conductive power bus tiers extending across the integrated circuit.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

MAR 29 2004

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
HALO-01-003B	10/782,358
Applicant: Tomoko Ogura et al.	
Filing Date: 02/19/04	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6255166	7/3/01	Ogura et al.	438	257	12/28/99
	6177318	1/23/01	Ogura et al.	438	267	10/18/99
	6477088	11/5/02	Ogura et al.	365	185.29	12/5/01
	6248633	6/19/01	Ogura et al.	438	267	10/25/99
	5933725	8/3/99	Kirsch et al.	438	239	5/27/98
	5973953	10/26/99	Yamashita et al.	365	63	3/11/98
	5459355	10/17/95	Kreifels	257	758	8/8/94

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
	0487468A2	11/14/91	European Patent App.	H01L	27/115		
DE	19824209A1	5/29/98	Germany	H01L	27/11		
EP	0871221A1	11/7/97	European Patent App	H01L	23/528		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.